

#18/F/D  
6/19/2  
Sushu

PATENT APPLICATION  
ATTORNEY DOCKET NO. Q60098

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Yoko HORIGUCHI

Appln. No.: 09/615,705

Confirmation No.: 4487

Filed: July 13, 2000

For: SEMICONDUCTOR INTEGRATED CIRCUIT



Group Art Unit: 2811

Examiner: O. Nadav

RECEIVED  
JUN 14 2002  
TECHNOLOGY CENTER 2800

**SUBMISSION OF CORRECTED FORMAL DRAWINGS**

Commissioner for Patents  
Washington, D.C. 20231

Sir:

Submitted herewith please find nine (9) sheets of corrected Formal Drawings. The Examiner is respectfully requested to acknowledge receipt of these corrected Formal Drawings.

The submitted drawings incorporate the proposed drawing changes approved in Paper Nos. 9 and 12.

Respectfully submitted,

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Date: June 13, 2002



Fig. 1

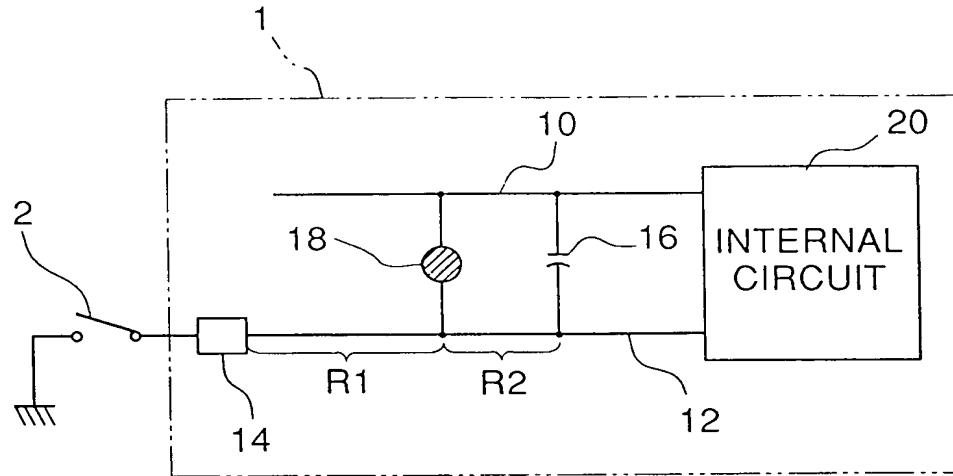


Fig. 2

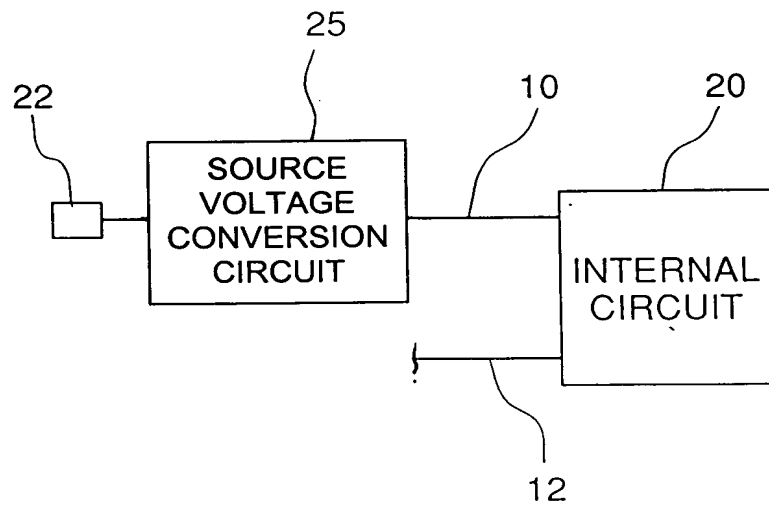


Fig. 3

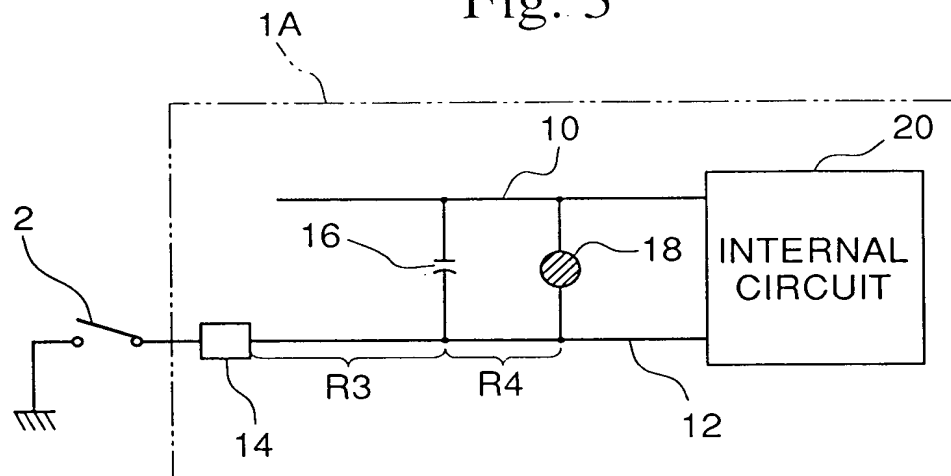


Fig. 4

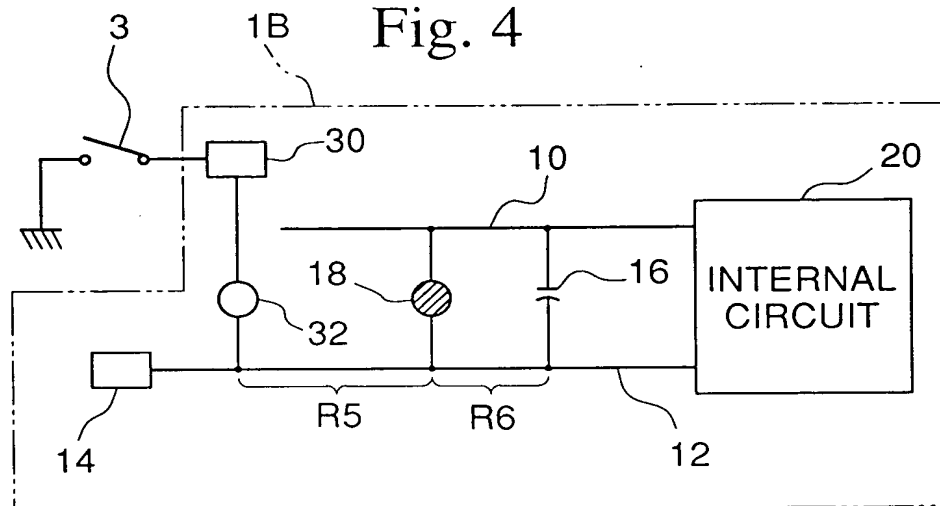


Fig. 5

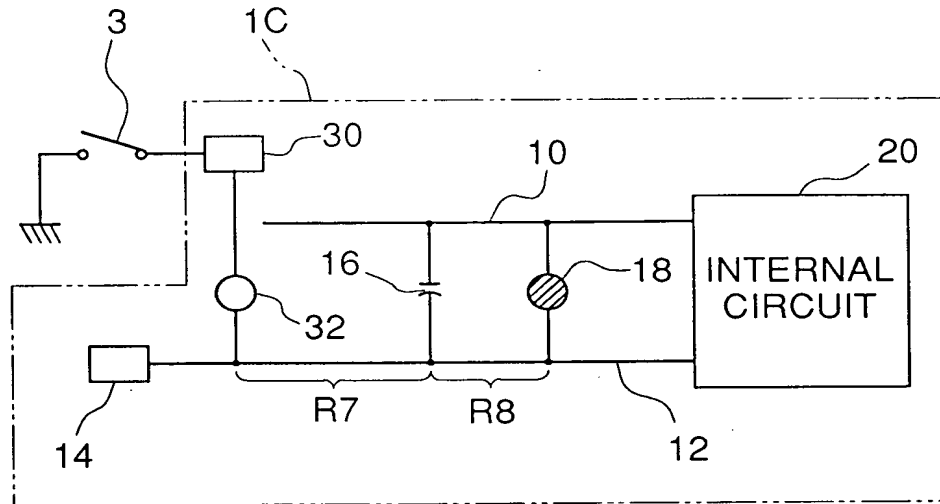


Fig. 6

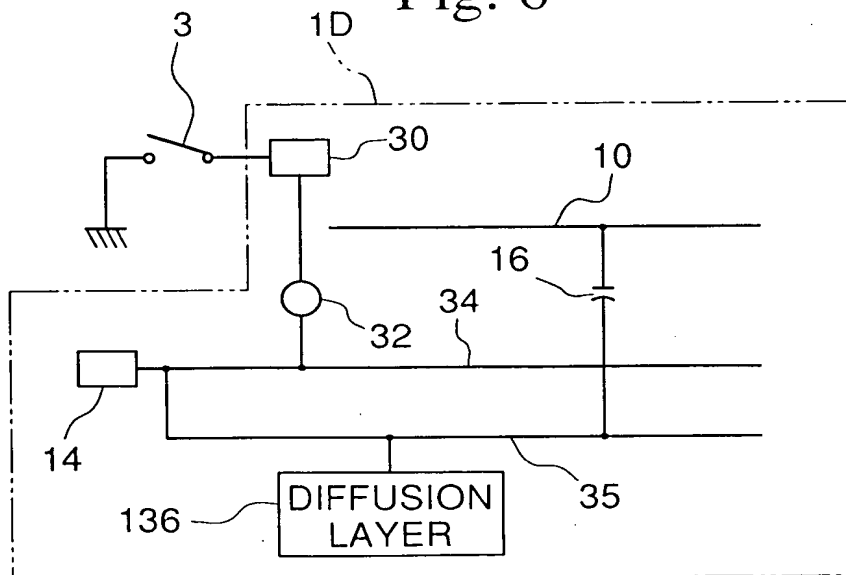


Fig. 7

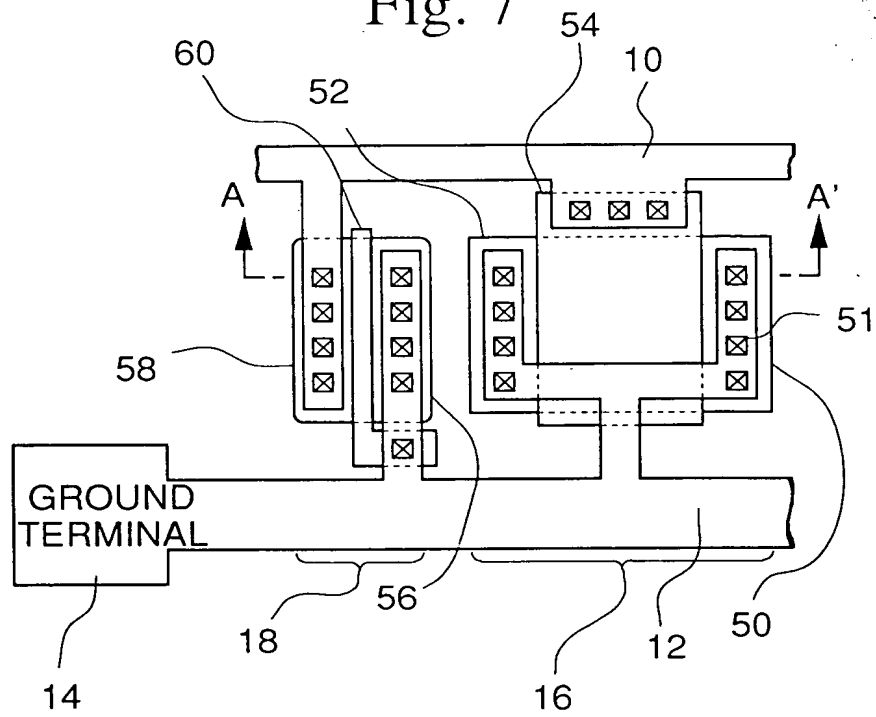


Fig. 8

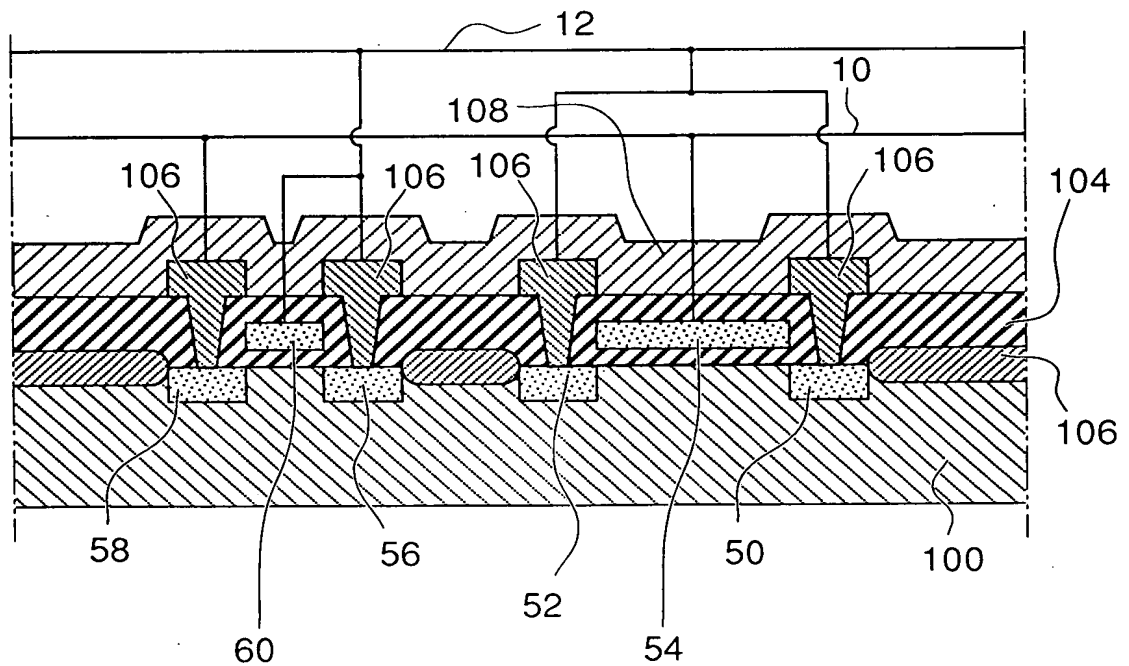


Fig. 9

30 INPUT/OUTPUT TERMINAL

34

74

72

52

54

10

B

B'

76

GROUND TERMINAL

14

32

18

70

16

12

50

51

[illegible]

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Fig. 11

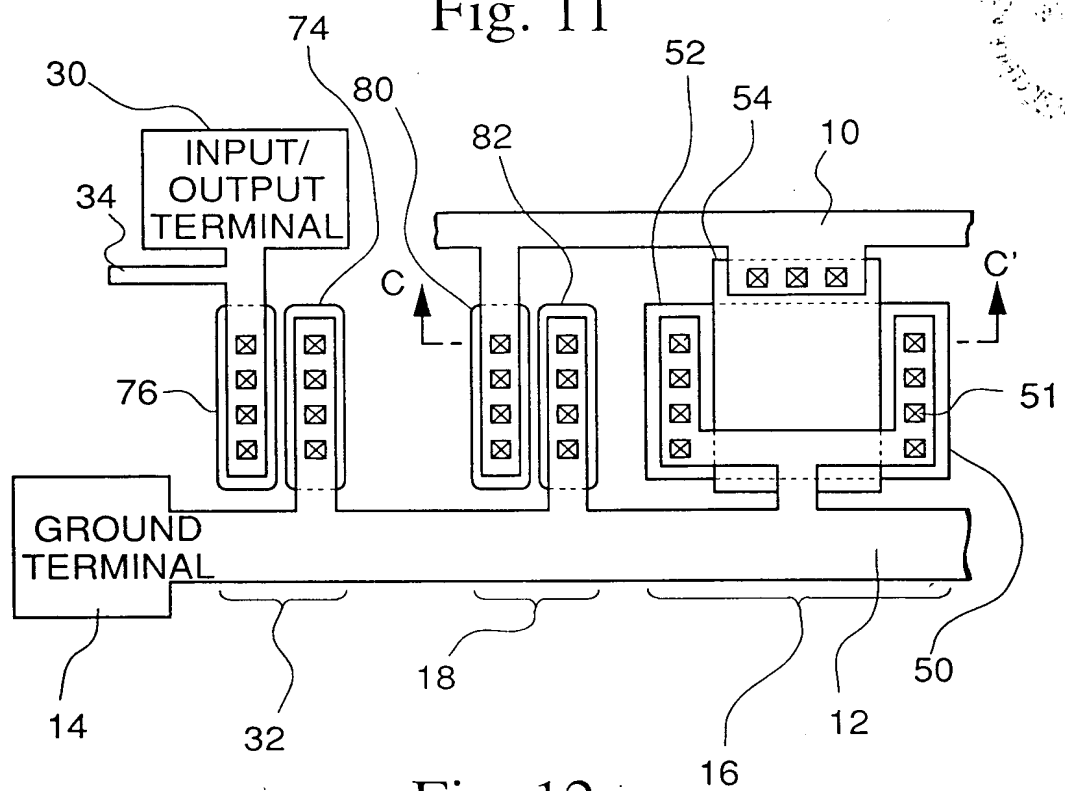


Fig. 12

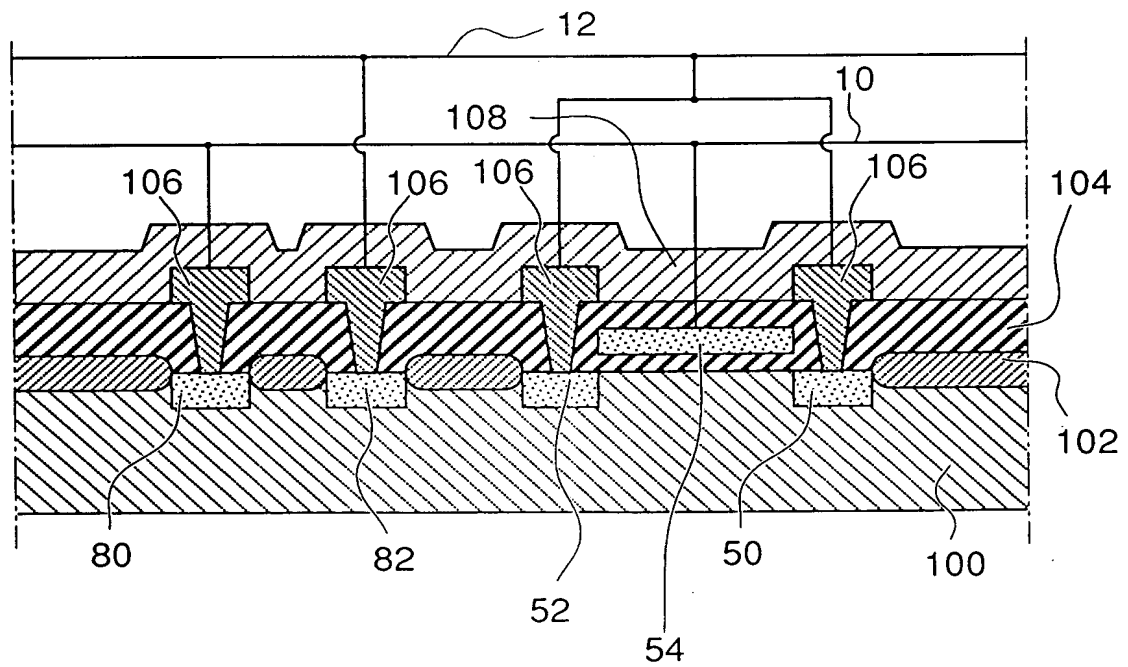


Fig. 14

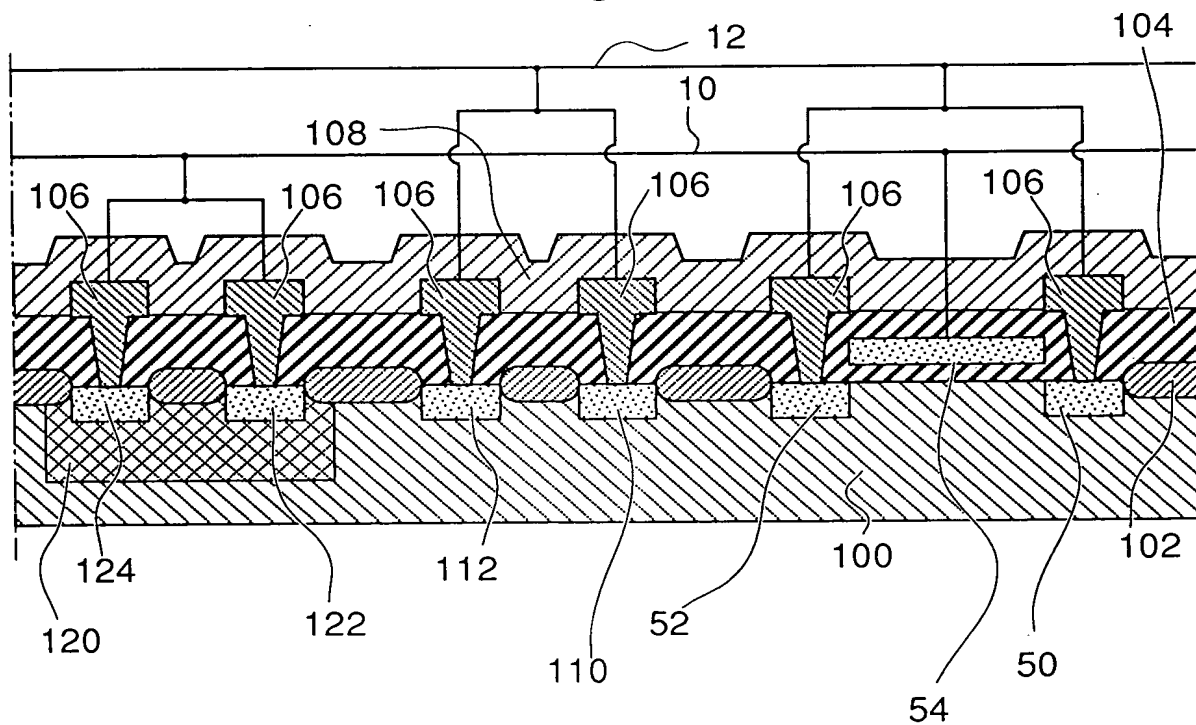




Fig. 15 PRIOR ART

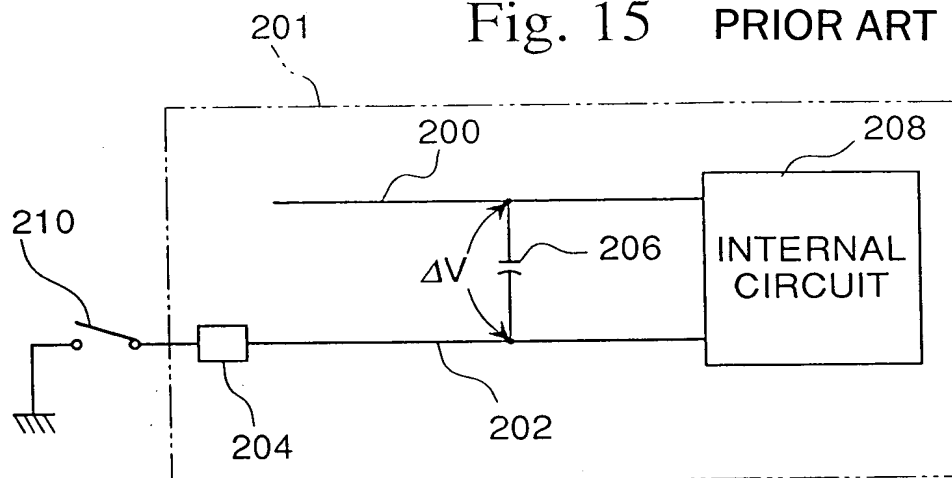


Fig. 16  
PRIOR ART

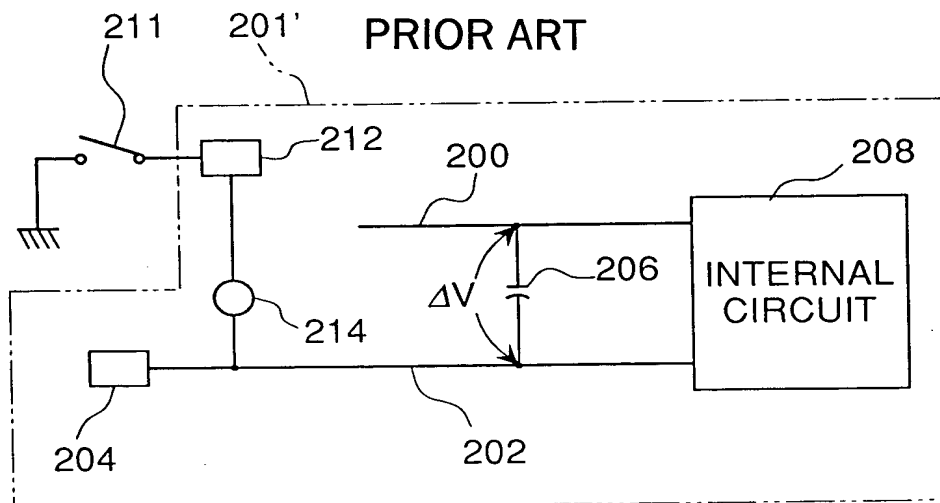


Fig. 17  
PRIOR ART

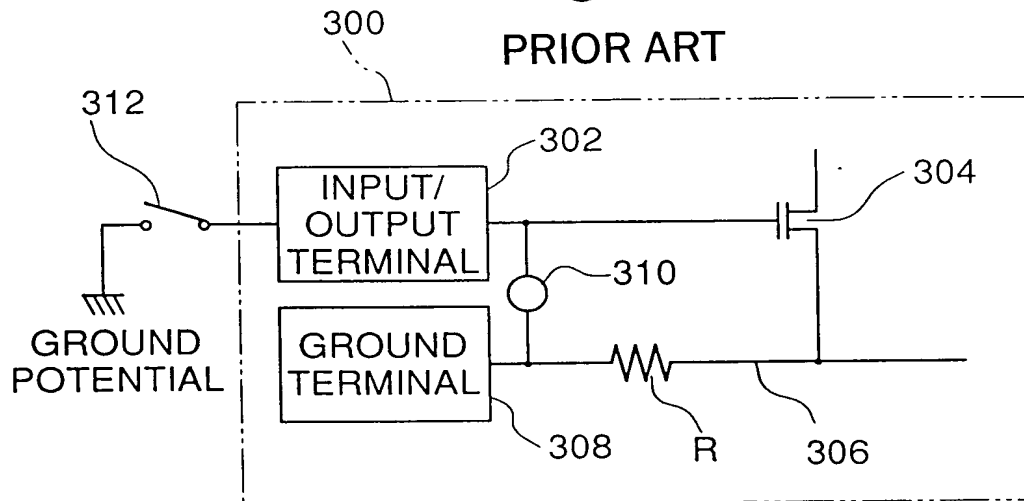


Fig. 18

